SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

WRITE PROTECTION IN THE I^2C and XI^2C EEPROM FAMILIES

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Among the non-volatile memories available today, the EEPROM is one of the most flexible memories which can be read, erased and written by byte or by block of bytes. This flexibility is appreciated in many applications but one aspect of flexibility in non-volatile memories is to not accept to store (and retain!) erroneous data. The EEPROM has therefore to offer an Erase/Write protect function in order to prevent erroneous Erase/Write cycles occuring. The ST24/25xxx serial EEPROMs compatible with the I^2C protocol, offer several features for protecting the data stored in the memory.

GLOBAL CONTROL OF THE ERASE/WRITE PROTECTION

Write Control Feature

The Write Control security feature ($\overline{WC}$ signal) is a global memory protection. In addition to the data line SDA and the serial clock SCL, the Write Control input signal can be driven to enable or inhibit the execution of an incoming Write command. When driven low ($\overline{WC}$=0), the EEPROM can be accessed (Erase/Write), when driven high ($\overline{WC}$=1), the EEPROM cannot be accessed (no Erase/Write). This $\overline{WC}$ input pin is driven by the bus master or by some other circuitry.

Dynamic Drive of the Write Control Signal

In order to get the best protection of data within the EEPROM, the bus master has to set the EEPROM in the Write protect mode; in this configuration, data stored in the memory cannot be modified. When the bus master has to write in the EEPROM, the bus master first deselects the memory protection (by driving low the $\overline{WC}$ pin), secondly writes and thirdly sets back the memory protection.

Address Counter Status

When using the Page Write instruction with the $\overline{WC}$ protection disabled ($\overline{WC}$ pin is driven low), the EEPROM internal address counter is incremented after each received byte and, in the case of the last received byte, it will set the EEPROM internal address counter to the right value for the first byte of the following Page Write command. When using the Page Write mode with the $\overline{WC}$ protection enabled ($\overline{WC}$ pin is driven high), the EEPROM internal address counter is incremented after each received byte except for the last received byte; the EEPROM internal address counter remains at the last received byte address.

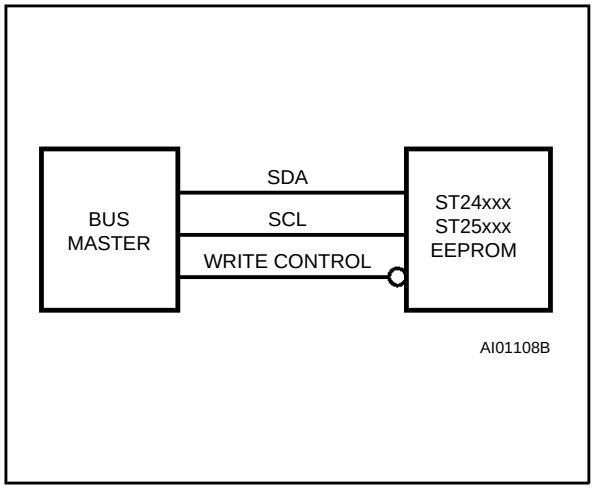
SELECTIVE CONTROL OF THE ERASE/WRITE PROTECTION

Write Protect Enable Feature

In addition to the Write Control feature, a second protection feature is offered on the ST24/25xxx devices with the help of the input pin PRE. This Protect Enable feature, associated to the PRE pin, is based on external and internal conditions, the external part is driven by the PRE pin and the internal part (software) allowing the definition of the size of the memory to be write controlled.

The memory area to be write protected is defined by an address pointer whose value is stored in the top byte of the memory (address 1FFh, 3FFh and 7FFh for ST24/25W04, ST24/25W08 and ST24/25W16 respectively). All the bytes between this top address and the address defined by the address pointer are protected if the PRE condition is met, as detailed further on. The maximum size of the protected memory is one half of the whole memory for ST24/25W04 and ST24/25W16, one quarter of the whole memory for ST24/25W08 (see Figure 2).

Figure 1. EEPROM Interface with Write Control Line



PRE Software Sequence

The complete sequence in order to protect an area is the following:

a. PRE pin is driven low (by the bus master)

b. Write the data inside the area to be write protected

c. Write the top byte. The Most Significant Bits (MSB) part of the top byte is the address pointer (see Figure 4 and Figure 5), the Least Significant Bits (LSB) are the control bits among which the Write Protect Disable Flag (bit 2) has to be set to '0' for enabling the write control feature.

d. PRE pin is driven high (by the bus master)

Data above the byte pointed by the address pointer are now write protected, they cannot be modified and are functionally equivalent to a ROM block.

Static and Dynamic PRE Control

The PRE pin may be driven dynamically by the bus master or wired to V_{CC} (or V_{SS}).

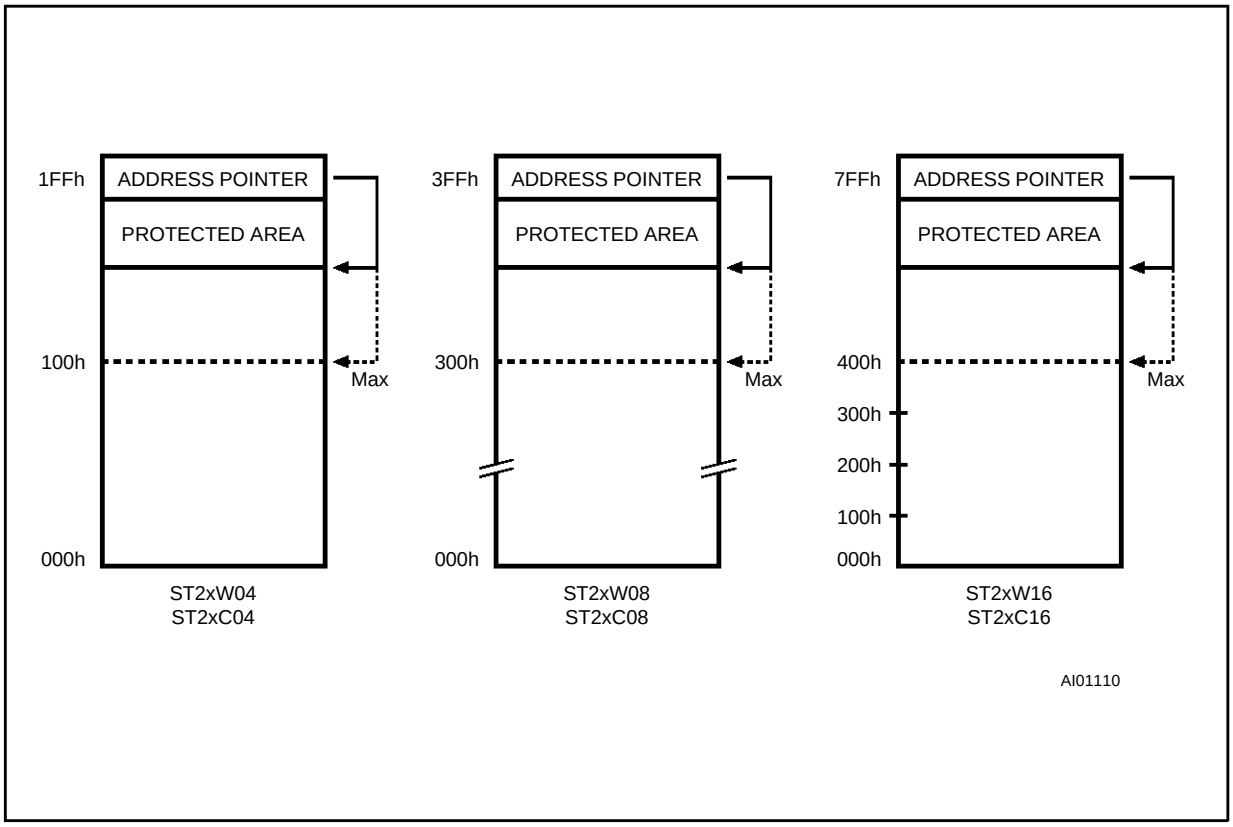
The dynamic drive from the bus master is performed in the same way that the $\overline{WC}$ pin driven. When the bus master has to write in the EEPROM, the bus master first deselects the memory protection, secondly writes and third sets back the PRE pin active. However, this dynamic mode does not make sense when the bus master controls the $\overline{WC}$ pin. The static drive of PRE is generally used with the help of a pull-up resistor, as shown in Figure 3.

The external pull-up resistor on PRE input pin allows the following steps:

– **Initialization of the secure area:** the EEPROM after insertion in the application board can still be driven externally by forcing the PRE pin to 0V (typically a short circuit to V_{SS} pin); under these conditions, the application designer may write application data (such as fabrication date, serial number, customer or dealer area, ...) and address pointer value which must stay unmodified when running the application. Once the PRE protected area is written, the external PRE short circuit is released.

– **When delivered to the end user**, the data written in the PRE protected area cannot be modified (the external pull up resistor on PRE disables the Erase/Write access to this area), only the complementary area inside the EEPROM can be fully accessed.

Figure 2. PRE Protected Areas



Leaving the PRE Mode

The PRE protected mode is active if the two following conditions are true: PRE pin is driven high and bit 2 of the protected memory Address Pointer (top location byte) is '0'. If one of these conditions is not true, the PRE protection is no longer active. In order to leave the PRE mode, the following sequence has to be run:

– PRE pin is driven low

– The Address Pointer (top location byte) is written with 0FFh to freeze the PRE protection and to reset the Address Pointer value.

More About the Address Pointer

The Address Pointer slightly differs with the ST24/25Wxx memory capacity. The following details the structure of this Address Pointer for each memory.

The ST24/25W04 and the ST24/25W08 have the same address pointer, as shown in Figure 4.

The address pointer consists of the 5 MSB (b7-b3) of the byte located at address 1FFh (ST24/25W04), 3FFh (ST24/25W08) with the 3 least significant bits being forced to '0' in all cases. Such an address pointer can define a protected area with a maximum size of 256 bytes, by steps of 8 bytes (because the 3 LSB are forced to '0').

The ST24/25W16 offers a larger address pointer, as shown in Figure 5.

The address pointer consists of the 4 MSB (b7-b4) of the byte located at address 7FFh, the 4 least significant bits being forced to '0' in all cases. Such an address pointer can define an address with a maximum range of 256 bytes, by steps of 16 bytes. In addition to this address pointer, two additional bits are selecting the block number (Block 0,1, 2 or 3) within which the (b7-b4) address pointer is defining the boundary of the protected area.

The size of the protected area is therefore extended up to 4 x 256 = 1024 bytes. These two additional bits (protect block) are driven by the logical level applied on input pins PB0,PB1.

Figure 3. Write Protect Enable Static Drive

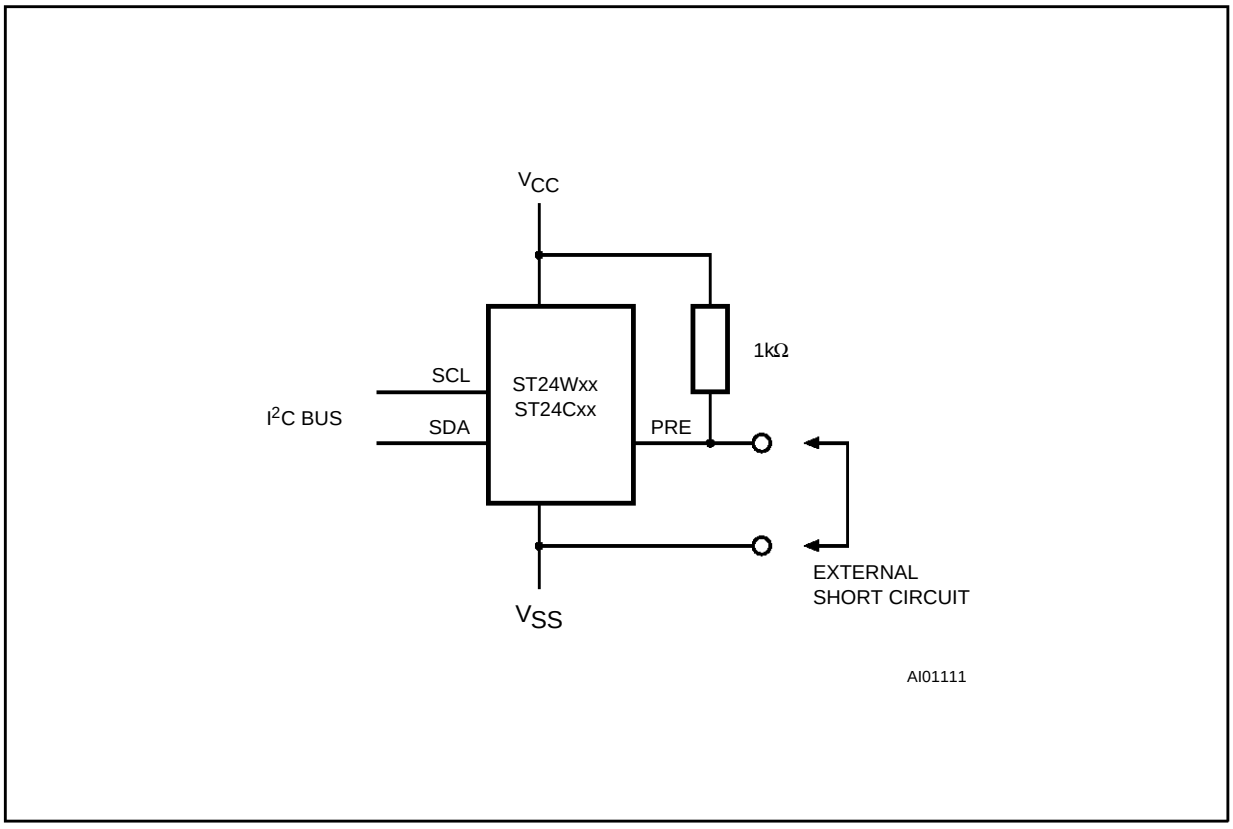


Figure 4. Address Pointer in 4K and 8K Devices

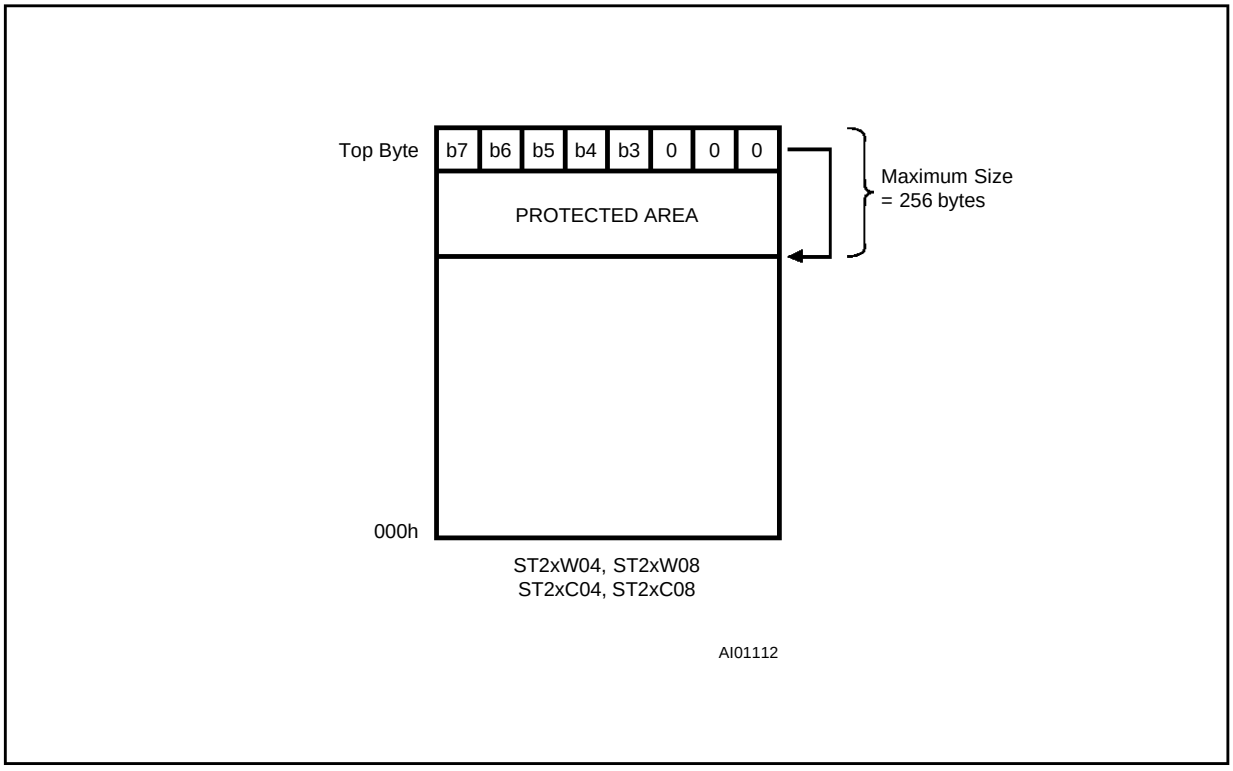
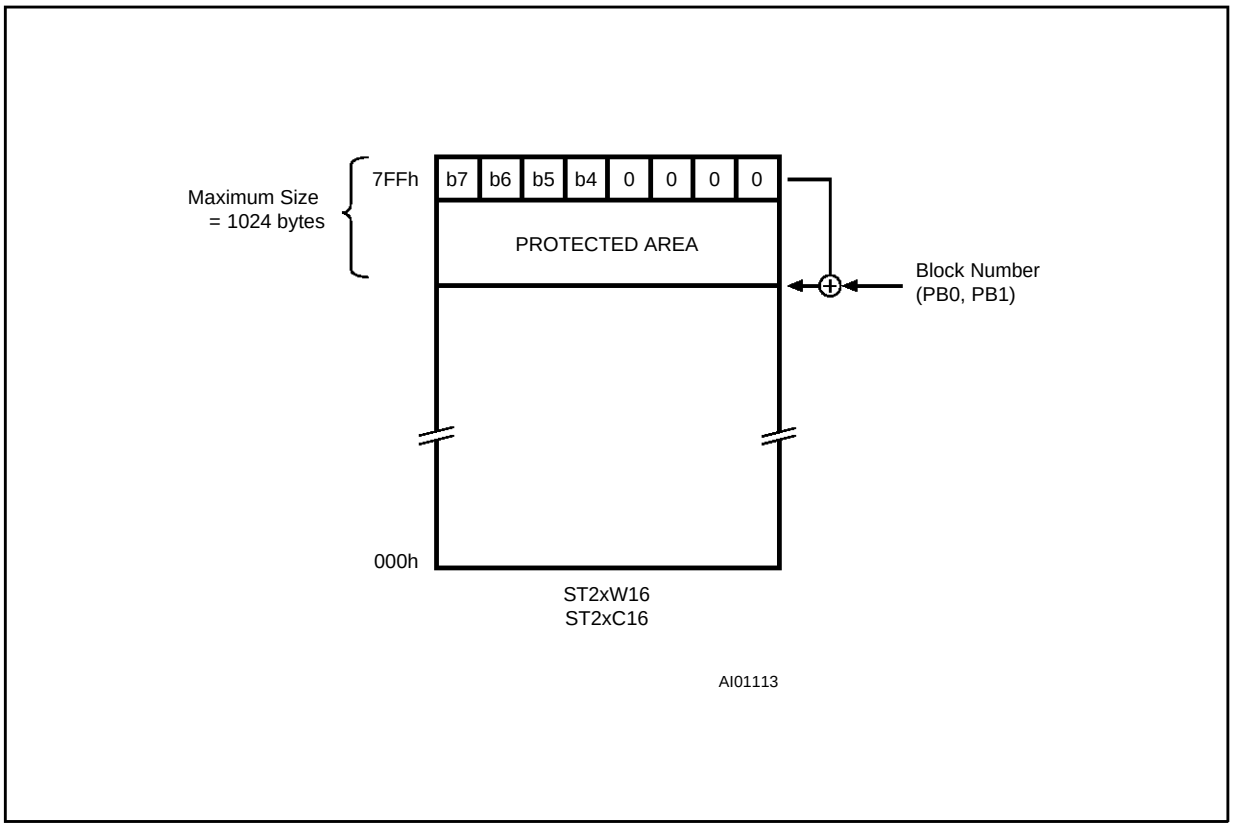


Figure 5. Address Pointer in 16K Device



PRE PROTECTION AND DEVICE PIN-OUT

The WriteProtect Enable feature is not available on all the ST24/25Cxx, ST24/25Wxx devices therefore the application designer should note that the pin-out of the ST24/25Cxx, ST24/25Wxx devices may differ for pins 1, 2 and 3. This device specific pin-out is related to the I^2C bus protocol when addressing devices of different memory size: for each ST24/25Cxx, ST24/25Wxx devices, the 4 MSB of the first byte (Device Select) are constant (1010), the following bits have a specific function dedicated to the size of the memory.

The following paragraph review the detail of each ST24/25Cxx, ST24/25Wxx device and the relationship between the pin-out and the PRE function.

ST24/25C01, ST24/25W01 (128 bytes)

The Device Select byte is composed of:

b7							b0
1	0	1	0	E2	E1	E0	R/W

where:

– E2 is the upper bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 2).

– E1 is the middle bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 1).

– E0 is the lower bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 0).

The Address Byte handles 7 significant bits, the MSB is a Don't Care bit (the ST24/25C01, ST24/25W01 is a 128 bytes memory, therefore addressed with only 7 bits). Pins 1, 2, 3 are E0, E1, E2 Chip Enable input pins (see Figure 6), this device does not offer the PRE feature.

ST24/25C02, ST24/25W02 (256 bytes)

The Device Select byte is composed of:

b7							b0
1	0	1	0	E2	E1	E0	R/W

where:

– E2 is the upper bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 2).

– E1 is the middle bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 1).

– E0 is the lower bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 0).

The Address Byte handles 8 significant bits (the ST24/25C02, ST24/25W02 is a 256 bytes memory, therefore addressed with 8 bits).

Pins 1, 2, 3 are E0, E1, E2 Chip Enable input pins (see Figure 6), this device does not offer the PRE feature.

ST24/25C04, ST24/25W04 (512 bytes)

The Device Select byte is composed of:

b7							b0
1	0	1	0	E2	E1	A8	R/W

where:

– E2 is the upper bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 2).

– E1 is the middle bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 1).

– A8 is the Memory Block number. A8 may also be considered as the upper bit of the address.

The Address Byte handles 8 significant bits (the ST24/25C04, ST24/25W04 is a 512 bytes memory splitted in 2 blocks of 256 bytes addressed with 8 bits). Pins 2, 3 are E1, E2 Chip Enable input pins (see Figure 6), pin 1 is the PRE input pin.

ST24/25C08, ST24/25W08 (1024 bytes)

The Device Select byte is composed of:

b7							b0
1	0	1	0	E2	A9	A8	R/W

where:

– E2 is the upper bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 2).

– A9,A8 is the Memory Block number. A9,A8 may also be considered as the upper bits of the address.

The Address Byte handles 8 significant bits (the ST24/25C08, ST24/25W08 is a 1024 bytes memory splitted in 4 blocks of 256 bytes addressed with 8 bits). Pin 3 is E2 Chip Enable input pin (see Figure 6), pin 2 is unused and pin 1 is the PRE input pin.

ST24/25C16, ST24/25W16 (2048 bytes)

The Device Select byte is composed of:

b7							b0
1	0	1	0	A10	A9	A8	R/W

where:

– A10,A9,A8 is the Memory Block number. A10,A9,A8 may also be considered as the upper bits of the address.

The Address Byte handles 8 significant bits (the ST24/25C16, ST24/25W16 is a 2048 bytes memory splitted in 8 blocks of 256 bytes addressed with 8 bits). Pin 1 is the PRE input pin, pins 2 and 3 are selecting the block of memory inside which the PRE pointer is defining the boundary of the protected area.

ST24/25E16, ST24/25E32, ST24/25E64

The Device Select byte is composed of:

b7							b0
1	0	1	0	E2	E1	E0	R/W

where:

– E2 is the upper bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 2).

– E1 is the middle bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 1).

– E0 is the lower bit of the Device Select code (this bit value must be identical to the value applied on pin Chip Enable 0).

The ST24/25E16 Address Bytes handle 16 bits (the 11 Lower bits are significant). Pins 1, 2, 3 are E0, E1, E2 Chip Enable input pins.

The ST24/25E32 Address Bytes handle 16 bits (the 12 Lower bits are significant). Pins 1, 2, 3 are E0, E1, E2 Chip Enable input pins.

The ST24/25E64 Address Bytes handle 16 bits (the 13 Lower bits are significant). Pins 1, 2, 3 are E0, E1, E2 Chip Enable input pins.

The ST24/25E16, ST24/25E32, ST24/25E64 do not offer the PRE feature.

Figure 6. Pin Connections Compatibility in the I²C and XI²C Product Families